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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,182	ROTHMAN ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/09/05&04/07/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings filed on 03/24/2004 have been approved by the Examiner.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 06/09/2005 and 04/07/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

5. Claims 11,21,41,47 and 50 are objected to because of the following informalities:

In claims 11,21,41,47 and 50, line 2, "said device data layout" should be changed to -- said device data layout information --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2,4-8,12-18,22-26 and 29-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchihori., US 6,516,389 B1.

Regarding claim 1, Uchihori teaches a method, comprising:

retrieving selected data (it is taught as prefetching data, col.5, lines 60-64 and col.13, lines 35-42) from one or more mass storage devices (it is taught as prefetching data from disk subsystem which comprises at least one disk device, col.5, lines 35-40), based at least in part on historical device access information of at least one requester of data (it is taught as prefetching data is based on the entries in the prediction table of Fig.9, step 35 in Fig.7 and col.13, lines 34-42. these entries are historical device access information of at least one requester of data).

Regarding claim 2, Uchihori further teaches comprising:

storing said selected data into cache memory (col.6, lines 22-28 and col.5, lines 63-64).

Regarding claim 4, Uchihori further teaches said historical device access information comprises at least in part, historical large block address (LBA) data generated by one or more data requests from said requester of data (col.13, lines 29-34 and Fig.9).

Regarding claim 5, Uchihori further teaches comprising:

receiving one or more requests for data, and determining if said one or more requests for data matches said selected data stored in cache memory (col.12, lines 21-24 and Fig.7 and col.7, lines 12-27).

Regarding claim 6, Uchihori further teaches comprising:

creating a requester profile (it is taught as creating the pre-fetch prediction table122, col.6, lines 43-47) by associating said requester of data with said historical device access information.

Regarding claim 7, Uchihori further teaches comprising:

updating said profile with additional device access information (it is taught as updating the contents of the prediction address field, col.7, lines 65 to col.8, lines 7).

Regarding claim 8, Uchihori further teaches said requester of data comprises information selected from a media access control (MAC) address, processor identification and user information (col.5, lines 28-40, when the host computer sends the data access request, the accessed data will transfer back to the host computer, therefore, the system needs to know the processor identification in order to transfer back the accessed data to the proper host computer which sent out the data access requester).

Regarding claim 12, Uchihori teaches an apparatus, comprising:

an integrated circuit (controller 123 as shown in Fig.1) that is capable of retrieving selected data (it is taught as prefetching data, col.5, lines 60-64 and col.13, lines 35-42) from one or more mass storage devices (it is taught as prefetching data from disk subsystem which comprises at least one disk device, col.5, lines 35-40), based at least in part on historical device access information of at least one requester of data (it is taught as prefetching data is based on the entries in the prediction table of Fig.9, step 35 in Fig.7 and col.13, lines 34-42. these entries are historical device access information of at least one requester of data).

Regarding claim 13, Uchihori further teaches said integrated circuit is further capable of storing said selected data into cache memory (col.6, lines 22-28 and col.5, lines 63-64).

Regarding claim 14, Uchihori further teaches said historical device access information comprises at least in part, historical large block address (LBA) data generated by one or more data requests from said requester of data (col.13, lines 29-34 and Fig.9).

Regarding claim 15, Uchihori further teaches said integrated circuit is further capable of receiving one or more requests for data; said integrated circuit is also capable of determining if said one or more requests for data matches said selected data stored in cache memory (col.12, lines 21-24 and Fig.7 and col.7, lines 12-27).

Regarding claim 16, Uchihori further teaches said integrated circuit is further capable of creating a requester profile (it is taught as creating the pre-fetch prediction table122, col.6, lines 43-47) by associating said requester of data with said historical device access information.

Regarding claim 17, Uchihori further teaches said integrated circuit is further capable of updating said requester profile with additional device access information from one or more said requesters of data (it is taught as updating the contents of the prediction address field, col.7, lines 65 to col.8, lines 7).

Regarding claim 18, Uchihori further teaches said requester of data comprises information selected from a media access control (MAC) address, processor

identification and user information (col.5, lines 28-40, when the host computer sends the data access request, the accessed data will transfer back to the host computer, therefore, the system needs to know the processor identification in order to transfer back the accessed data to the proper host computer which sent out the data access requester).

Regarding claim 22, Uchihori teaches an article, comprising:

a storage medium having stored thereon instructions (Uchihori teaches the readout access execution means, see col.1, lines 62-64, it implies that instructions stored in the storage medium has been executed) that when executed by a machine result in the following:

retrieving selected data (it is taught as prefetching data, col.5, lines 60-64 and col.13, lines 35-42) from one or more mass storage devices (it is taught as prefetching data from disk subsystem which comprises at least one disk device, col.5, lines 35-40) by an integrated circuit (controller 123 as shown in Fig1), based at least in part on historical device access information of at least one requester of data (it is taught as prefetching data is based on the entries in the prediction table of Fig.9, step 35 in Fig.7 and col.13, lines 34-42. these entries are historical device access information of at least one requester of data).

Regarding claim 23, Uchihori further teaches said integrated circuit is capable of storing said selected data into cache memory (col.6, lines 22-28 and col.5, lines 63-64).

Regarding claim 24, Uchihori further teaches said integrated circuit is capable of receiving one or more requests for data; said integrated circuit is also capable of determining if said one or more requests for data matches said selected data stored in cache memory (col.12, lines 21-24 and Fig.7 and col.7, lines 12-27).

Regarding claim 25, Uchihori further teaches said integrated circuit is capable of creating a requester profile (it is taught as creating the pre-fetch prediction table122, col.6, lines 43-47) by associating said requester of data with said historical device access information.

Regarding claim 26, Uchihori further teaches said integrated circuit is capable of updating said profile with additional device access information (it is taught as updating the contents of the prediction address field, col.7, lines 65 to col.8, lines 7).

Regarding claim 29, Uchihori teaches a system, comprising:

a controller card (it is taught as disk control device 12 as shown in Fig.1) including an integrated circuit, the controller card being capable of being coupled to a bus (disk control device is coupled to SCSI bus 30), the integrated circuit being capable of retrieving selected data (it is taught as prefetching data, col.5, lines 60-64 and col.13, lines 35-42) from one or more mass storage devices external to said integrated circuit (it is taught as prefetching data from disk subsystem which comprises at least one disk

device such as HDD, col.5, lines 35-40), based at least in part on historical device access information of at least one requester of data (it is taught as prefetching data is based on the entries in the prediction table of Fig.9, step 35 in Fig.7 and col.13, lines 34-42. these entries are historical device access information of at least one requester of data).

Regarding claim 30, Uchihori further teaches said integrated circuit is further capable of storing said selected data into cache memory (col.6, lines 22-28 and col.5, lines 63-64).

Regarding claim 31, Uchihori further teaches said requester of data comprises one or more workstations capable of exchanging commands and data with said integrated circuit (Uchihori only teaches on host computer, it is well known in the art that the prefetching mechanism can be implemented if multiple hosts are connected to the disk subsystem).

Regarding claim 32, Uchihori further teaches each said workstation capable of generating at least one of a media access control (MAC) address, processor identification and user information information (col.5, lines 28-40, when the host computer sends the data access request, the accessed data will transfer back to the host computer, therefore, the system needs to know the processor identification in order

to transfer back the accessed data to the proper host computer which sent out the data access requester).

Regarding claim 33, Uchihori further teaches said one or more mass storage devices comprising a storage array (col.5, lines 35-40).

Regarding claim 34, Uchihori further teaches said integrated circuit is further capable of receiving one or more requests for data; said integrated circuit is also capable of determining if said one or more requests for data matches said selected data stored in cache memory (col.12, lines 21-24 and Fig.7 and col.7, lines 12-27).

Regarding claim 35, Uchihori further teaches said integrated circuit is further capable of creating a requester profile (it is taught as creating the pre-fetch prediction table122, col.6, lines 43-47) by associating said requester of data with said historical device access information

Regarding claim 36, Uchihori further teaches said integrated circuit is further capable of updating said requester profile with additional device access information from one or more said requesters of data (it is taught as updating the contents of the prediction address field, col.7, lines 65 to col.8, lines 7).

8. Claims 39-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Harmer., US 2002/0152354 A1.

Regarding claim 39, Harmer teaches a method, comprising:

retrieving device data layout information (it is taught as retrieving directory entries such as a file name, a file type etc., Fig.6 and section 0043) from one or more mass storage devices (section 0013 and section 0028) by an integrated circuit (it is taught as a disk drive controller 72), and storing said device data layout information in cache memory by said integrated circuit (it is taught as the file system data is cached, section 0013 and section 0038, last four lines and section 0039).

Regarding claim 40, Harmer teaches the integrated circuit is further capable of responding to a request for data (it is taught as receiving a request to read a portion of a file) by determining the location of said data on said one or more mass storage devices (it is taught as determining where that file is located on the disk before it can even try to read the file) by performing selected disk access operations on said data layout information in said cache memory (it is taught as reading through the file names in a directory to try to find a match for the file name that had been requested; section 0030, lines 1-6).

Regarding claim 41, Harmer further teaches said device data layout information comprises a file system type selected from a file allocation (FAT) file system and a new technology file system (NTFS) type (section 0037 and 0038).

Regarding claim 42, Harmer teaches an article, comprising:

a storage medium having stored thereon instructions (Harmer teaches a host computer having system BIOS ROM 13, Fig.1) that when executed by a machine result in the following:

retrieving device data layout information (it is taught as retrieving directory entries such as a file name, a file type etc., Fig.6 and section 0043) from one or more mass storage devices (section 0013 and section 0028) by an integrated circuit (it is taught as a disk drive controller 72), and storing said device data layout information in cache memory by said integrated circuit (it is taught as the file system data is cached, section 0013 and section 0038, last four lines and section 0039).

Regarding claim 43, Harmer teaches the integrated circuit is further capable of responding to a request for data (it is taught as receiving a request to read a portion of a file) by determining the location of said data on said one or more mass storage devices (it is taught as determining where that file is located on the disk before it can even try to read the file) by performing selected disk access operations on said data layout information in said cache memory (it is taught as reading through the file names in a directory to try to find a match for the file name that had been requested; section 0030, lines 1-6).

Regarding claim 44, Harmer teaches a system, comprising:

a controller card (it is taught as hard disk drive 56) including an integrated circuit, the controller card being capable of being coupled to a bus (hard disk drive is coupled to a peripheral bus 52), the integrated circuit being capable exchanging commands and data with one or more mass storage devices (the disk drive controller 72 controls the hard disk drive operations such as read or write, section 0028, last three lines), said integrated circuit being further capable of retrieving device data layout information (it is taught as retrieving directory entries such as a file name, a file type etc., Fig.6 and section 0043) from one or more mass storage devices (section 0013 and section 0028) by an integrated circuit (it is taught as a disk drive controller 72), and storing said device data layout information in cache memory by said integrated circuit (it is taught as the file system data is cached, section 0013 and section 0038, last four lines and section 0039).

Regarding claim 45, Harmer further teaches said one or more mass storage devices comprising a storage array (Harmer teaches mass memory storage peripheral computer device 56 is a hard disk drive and memory storage 58 is the hard disk drive memory storage, it is well know in the art that mass memory storage device can be implemented as a storage array).

Regarding claim 46, Harmer teaches said integrated circuit is further capable of responding to a request for data (it is taught as receiving a request to read a portion of a file) by determining the location of said data on said one or more mass storage devices (it is taught as determining where that file is located on the disk before it can even try to

read the file) by performing selected disk access operations on said data layout information in said cache memory (it is taught as reading through the file names in a directory to try to find a match for the file name that had been requested; section 0030, lines 1-6).

Regarding claim 47, Harmer further teaches said device data layout information comprises a file system type selected from a file allocation (FAT) file system and a new technology file system (NTFS) type (section 0037 and 0038).

Regarding claim 48, Harmer teaches an apparatus, comprising:

an integrated circuit capable of retrieving device data layout information (it is taught as retrieving directory entries such as a file name, a file type etc., Fig.6 and section 0043) from one or more mass storage devices (section 0013 and section 0028) by an integrated circuit (it is taught as a disk drive controller 72), and storing said device data layout information in cache memory by said integrated circuit (it is taught as the file system data is cached, section 0013 and section 0038, last four lines and section 0039).

Regarding claim 49, Harmer teaches said integrated circuit is further capable of responding to a request for data (it is taught as receiving a request to read a portion of a file) by determining the location of said data on said one or more mass storage devices (it is taught as determining where that file is located on the disk before it can even try to read the file) by performing selected disk access operations on said data layout

information in said cache memory (it is taught as reading through the file names in a directory to try to find a match for the file name that had been requested; section 0030, lines 1-6).

Regarding claim 50, Harmer further teaches said device data layout information comprises a file system type selected from a file allocation (FAT) file system and a new technology file system (NTFS) type (section 0037 and 0038).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uchihori., US 6,516,389 B1, in view of Mogi et al., US 2004/0193807 A1.

Regarding claim 3, Uchihori teaches the claimed invention as claimed in claim 1 as shown above, Uchihori does not further teach said historical device access information comprises, at least in part, device identification information of one or more said mass storage devices, Uchihori only teaches that pre-fetch prediction table contains a plurality of entries and each entry includes an area address field and a prediction address field (col.6, lines 59-67). However, Mogi teaches said historical

device access information (entries in the prefetching method 720 as shown in Fig.18) comprises, at least in part, device identification information of one or more said mass storage devices (Fig. 18, device identification information of one or more said mass storage devices is taught as the drive ID, entry 723, section 0144).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Mogi into Uchihori's system such as said historical device access information comprises, at least in part, device identification information of one or more said mass storage devices because the access performance of the storage device is enhanced by using the prefetching method of Mogi as shown in Fig.18 (see Mogi, section 0005, last five lines).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor (both references teaches prefetch method and prefetch entires). This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

11. Claims 9-11,19-21,27-28 and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchihori., US 6,516,389 B1, in view of Harmer ., US 2002/0152354 A1.

Regarding claims 9,19,27 and 37, Uchihori teaches the claimed invention as claimed in independent claims as shown above, Uchihori does not further teach retrieving device data layout information from one or more said mass storage devices and storing said device data layout information in said cache memory. However,

Harmer teaches retrieving device data layout information (it is taught as directory entries such as a file name, a file type etc., Fig.6 and section 0043) from one or more said mass storage devices (section 0013 and section 0028) and storing said device data layout information in said cache memory (it is taught as the file system data is cached, section 0013 and section 0038, last four lines and section 0039).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Harmer into Uchihori's system such as retrieving device data layout information from one or more said mass storage devices and storing said device data layout information in said cache memory because the overall performance of the computer system is improved due to less I/O being required to satisfy a file read or write request from an application program and it also helps to reduce the cost of the mass storage peripheral device (see Harmer, section 0050).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor (both references teaches storing data from the hard disk drive to the cache memory). This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claims 10, 20, 28 and 38, Harmer further teaches comprising:

responding to a request for data (it is taught as receiving a request to read a portion of a file) by determining the location of said data on said one or more mass storage devices (it is taught as determining where that file is located on the disk before

it can even try to read the file) by performing selected disk access operations on said data layout information in said cache memory (it is taught as reading through the file names in a directory to try to find a match for the file name that had been requested; section 0030, lines 1-6).

Regarding claims 11 and 21, Harmer further teaches said device data layout information comprises a file system type selected from a file allocation (FAT) file system and a new technology file system (NTFS) type (section 0037 and 0038).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Idei et al	US 2004/0117398 A1
Okayasu	US 2002/0002658 A1
Shatil et al	US 6728840 B1

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jasmine Song

Patent Examiner

July 21, 2006